INTERPOLATING CIRCUIT FOR NORMAL VECTOR IN GRAPHIC PROCESSOR

Patent number: JP1204191
Publication date: 1989-08-16
Inventor: SAITO ATSUSHI; TOTSUKA TAKUSHI; SHIBATA KOICHI
Applicant: SEIKO INSTR & ELECTRONICS
Classification:
- international: G06F15/72
- european:
Application number: JP19880028167 19880209
Priority number(s): JP19880028167 19880209

Abstract of **JP1204191**

PURPOSE:To reduce the quantity of normal vector information and to compress a luminance converting table by dither-processing the output of a normal vector interpolating circuit with a dither processing circuit once. CONSTITUTION:An address generating circuit 35 prepares the position information of a picture element group and a control circuit 30 synchronizes to it and successively prepares the normal vector information having respective picture elements. The output of a normal vector interpolating circuit 31 to execute the vector interpolation operation by the normal vector is inputted to a dither processing circuit 32, the processing based on the dither method is executed and the result is made into the input of a luminance converting table 33. Thus, the input information quantity of the luminance converting table 33 can be reduced and the size of the luminance converting table 33 can be compressed.